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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/853,335
Filing Date: May 11, 2001
Appellant(s): STRONGIN ET AL.

Mark W. Sincell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/18/05.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-13 and 15-57. The status of the claims is substantially correct except for the statement that "claims 16-19 and 21-29 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Moriarty in view of Kao, et al (U.S. Patent No. 6,651,168)". The previous examiner did not include claim 20 in the heading of the rejection, however claim 20 was included in the body of the rejection. As such, Claims 16-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Moriarty in view of Kao, et al.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: (D) Whether claims 16-20 are obvious over Moriarty in view of Kao.

(7) Grouping of Claims

The rejection of claims 1-13 and 15-57 stand or fall together because appellant's brief include a statement that this grouping of claims stand or fall together. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,651,168	Kao et al	11-2003
6,636,921	Scholhamer et al	10-2003
6,446,149	Moriarty et al	9-2002
6,356,983	Parks	3-2002

Microsoft Press Computer Dictionary Third edition 1997 page 428

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-8, 10-15 and 30-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty et al. (USPN 6,446,149; Moriarty).

As per claim 1, Moriarty discloses a bus interface logic (bridge) configured with a storage location (address space / semaphore memory cell; abstract) configured to store a master mode bit (semaphore memory cell; abstract; col. 2, lines 16-23), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46).

As per claim 2, Moriarty discloses the bus interface logic of claim 1 further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 4, Moriarty discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the bus interface logic is configured to exchange data only with the one or more addresses (col. 11, lines 35-46).

As per claim 5, Moriarty discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (e.g. col. 11, lines 20-25), wherein the bus interface logic is configured to exchange data only within the address range.

As per claim 6, Moriarty discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 9, lines 44-47).

As per claim 7, Moriarty discloses a computer system, comprising: a master device (busmaster) configured to set and reset a master mode bit (read/write; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67); and one or more bus interface logics (bridges), each configured with a storage location configured to store the master mode bit (address space/ semaphore memory cell; abstract; col. 2, lines 16-23), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46).

As per claim 8, Moriarty computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 56-61; col. 11, lines 37-44).

As per claim 10, Moriarty discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 11, Moriarty discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (col. 11, lines 20-25), wherein the one or more bus interface logics are configured to exchange data only within the address range.

As per claims 12 and 14, Moriarty discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 13, Moriarty discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 9, lines 44-47).

As per claim 15, Moriarty inherently discloses a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set. In that the bridges of the Moriarty system functions for normal data exchange between plurality of bus masters and targets when the master mode bit is not set. However, when the master mode bit is set, only the bus master with exclusive access as indicated by the master mode bit being set would be able to exchange data through the bridge(s).

As per claims 30 and 47, Moriarty discloses a method and computer instructions (algorithm; col.8, lines 1 et seq.) of operating a computer system, the method comprising: setting a master mode bit for a bus interface logic (read; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67); passing a data request through the bus interface logic only for a specified device (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46); receiving data in response to the data request from the specified device (col. 2,

lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46) and resetting the master mode bit (write; col. 8, lines 18-67).

As per claims 31 and 48, Moriarty further discloses setting a master mode bit in another bus interface logic (col. 12, lines 52-56); and passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 10, lines 21-67).

As per claims 32 and 49, Moriarty further discloses the method wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic (e.g. col. 7, lines 28-34); and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 10, lines 21-67; col. 11, lines 35-46).

As per claims 33 and 50, Moriarty further discloses the method comprising:
making an attempt to access the bus interface logic; and rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (read/busy; e.g. col. 7, lines 28-34) .

As per claims 34 and 51, Moriarty further discloses the method comprising: resetting (write) the master mode bit; and flushing buffers of the bus interface logic in response to resetting the master mode bit (col. 9, lines 44-51; col. 11, lines 35-46).

As per claims 35 and 52, Moriarty discloses the method of claim 34, further comprising: making an attempt to access the bus interface logic; and accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device

or the specified device, after the master mode bit is reset (read by another master; e.g. col. 7, lines 28-34; col. 9, lines 56-61).

As per claims 36 and 53, Moriarty further discloses the method comprising: storing one or more address locations along with the master mode bit for the bus interface logic (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 37 and 54, Moriarty further discloses the method comprising: restricting data transmissions only to the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 38 and 55, Moriarty further discloses the method comprising: restricting data transmissions only to within an address range defined by the one or more address locations (e.g. col. 11, lines 20-25).

As per claims 39 and 56, Moriarty further discloses the method comprising: restricting data transmissions from the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 40 and 57, Moriarty further discloses the method comprising: restricting data transmissions from within an address range defined by the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 41, Moriarty discloses a computer system, comprising: means (address space/semaphore memory cells) for storing an indicator of a master mode; means (bridge) for restricting data transfers when the indicator of the master mode is set; means (address space/semaphore memory cells; busmaster(s)) for resetting the indicator of the master mode (write; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 42, Moriarty discloses a computer system, comprising: means (busmaster; read) for setting a master mode bit for a bus interface logic; means (bridge) for passing a data request through the bus interface logic only for a specified device; means (bridge; gateway) for receiving data in response to the data request from the specified device; and means (busmaster; write) for resetting the master mode bit (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 43, Moriarty discloses the computer system of claim 42, further comprising: means for setting a master mode bit in another bus interface logic (col. 12, lines 52-56); and means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 10, lines 21-67).

As per claim 44, Moriarty discloses the computer system of claim 42, further comprising: means (bridge) for rejecting (busy) an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 45, Moriarty discloses the computer system of claim 42, further comprising: means for resetting the master mode bit (busmaster; write); and means for flushing buffers of the bus interface logic in response to resetting the master mode bit (col. 9, lines 44-51; col. 11, lines 35-46).

As per claim 46, Moriarty discloses the computer system of claim 45, further comprising: means for accessing the bus interface logic in response to making an attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (read by another master; e.g. col. 7, lines 28-34; col. 9, lines 56-61).

Claims 1-2, 4-8, 10-15, 30-31 and 47-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Parks (USPN 6,356,983).

As per claims 1, 30 and 47, Parks discloses system and method comprising: a bus interface logic (repeater and repeater control & status registers; fig. 3, 4 or 10) configured with a storage location (status registers or ID registers) configured to store a master mode bit (initiator ID; col. 8, lines 26-28 and 40-67), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 8, lines 26-28 and 40-67).

As per claim 2, Parks discloses the bus interface logic of claim 1, further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 4, 31 and 48, Parks discloses wherein the storage location is further configured to store one or more addresses (col. 8, lines 26-28 and 40-67), and wherein the bus interface logic is configured to exchange data only with the one or more addresses (col. 8, lines 26-28 and 40-67).

As per claim 5, Parks discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (ID0-ID7 or ID0-ID15), wherein the bus interface logic is configured to exchange data only within the address range.

As per claim 6, Parks discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (ID0-ID7 or ID0-ID15), and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 14, lines 14-51).

As per claim 7, Parks discloses a computer system, comprising: a master device (e.g. initiator) configured to set and reset a master mode bit (initiator ID; col. 8, lines 26-28 and 40-67); and one or more bus interface logics, each configured with a storage location configured to store the master mode bit (repeater and repeater control & status registers; fig. 3, 4 or 10; initiator ID; col. 8, lines 26-28 and 40-67), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 8, lines 26-28 and 40-67).

As per claim 8, Parks computer system of claim 7, wherein the bus interface logics are further

configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 10, Parks discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 8, lines 26-28 and 40-67).

As per claim 11, Parks discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (ID0-ID7 or ID0-ID15), wherein the one or more bus interface logics are configured to exchange data only within the address range (col. 8, lines 26-28 and 40-67).

As per claims 12 and 14, Parks discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (e.g. col. 8, lines 26-28 and 40-67).

As per claim 13, Parks discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 14, lines 14-51).

As per claim 15, Parks discloses the computer system of claim 7, further comprising: a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set (col. 8, lines 26-28 and 40-67 and col. 14, lines 14-51).

Claims 1-15 and 30-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Scholhamer et al. (USPN 6636921; Scholhamer).

As per claims 1 and 3, Scholhamer discloses a bus interface logic (col. 7, lines 3-10) configured with a storage location (303) configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 2, Scholhamer discloses the bus interface logic of claim 1, further configured to flush output buffers in response to the master mode bit being reset

As per claim 4, Scholhamer discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 9, lines 19-33), and

wherein the bus interface logic is configured to exchange data only with the one or more addresses.

As per claim 5, Scholhamer discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (Node Presence vector), wherein the bus interface logic is configured to exchange data only within the address range (col. 9, lines 19-33).

As per claim 6, Scholhamer discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 16, lines 4-6).

As per claims 7 and 9, Scholhamer discloses a computer system, comprising: a master device (e.g. Nodes and Node Processors) configured to set and reset a master mode bit (col. 7, lines 3-10); and one or more bus interface logics, each configured with a storage location configured to store the master mode bit (col. 6, lines 35-67; col. 7, lines 3-10), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 8, Scholhamer discloses the computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset.

As per claim 10, Scholhamer discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 9, lines 19-33).

As per claim 11, Scholhamer discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (Node Presence vector), wherein the one or more bus interface logics are configured to exchange data only within the address range (col. 9, lines 19-33).

As per claims 12 and 14, Scholhamer discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (col. 6, lines 35-67; col. 7, lines 3-10).

As per claim 13, Scholhamer discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 16, lines 4-6).

As per claim 15, Scholhamer discloses the computer system of claim 7, further comprising: a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set (col. 9, lines 54-55).

As per claims 30 and 47, Scholhamer discloses a method and computer instructions (operations) of operating a computer system, the method comprising: setting a master mode bit for a bus interface logic (col. 6, lines 35-67; col. 7, lines 3-10); passing a data request through the bus interface logic only for a specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5); receiving data in response to the data request from the specified device (col. 9, lines

919-33; col. 12, lines 50-53; see also Table 5) and resetting the master mode bit (col. 7, lines 3-10).

As per claims 31 and 48, Scholhamer further discloses setting a master mode bit in another bus interface logic; and passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claims 32 and 49, Scholhamer further discloses the method wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5); and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claims 33 and 50, Scholhamer further discloses the method comprising: making an attempt to access the bus interface logic; and rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (request and retry; col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5) .

As per claims 34 and 51, Scholhamer further discloses the method comprising: resetting the master mode bit; and flushing buffers of the bus interface logic in response to resetting the master mode bit.

As per claims 35 and 52, Scholhamer discloses the method of claim 34, further comprising: making an attempt to access the bus interface logic; and accessing the bus interface

logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (uncached; col. 12, lines 14-15).

As per claims 36 and 53, Scholhamer further discloses the method comprising: storing one or more address locations along with the master mode bit for the bus interface logic (col. 6, lines 35-67; col. 7, lines 3-10).

As per claims 37 and 54, Scholhamer further discloses the method comprising: restricting data transmissions only to the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 38 and 55, Scholhamer further discloses the method comprising: restricting data transmissions only to within an address range defined by the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 39 and 56, Scholhamer further discloses the method comprising: restricting data transmissions from the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 40 and 57, Scholhamer further discloses the method comprising: restricting data transmissions from within an address range defined by the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claim 41, Scholhamer discloses a computer system, comprising: means (303) for storing an indicator of a master mode; means (e.g. 300) for restricting data transfers when the

indicator of the master mode is set; means (e.g. 301) for resetting the indicator of the master mode (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 42, Scholhamer discloses a computer system, comprising:
means (301) for setting a master mode bit for a bus interface logic;
means (301) for passing a data request through the bus interface logic only for a specified device;
means (301) for receiving data in response to the data request from the specified device; and
means (301) for resetting the master mode bit (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 43, Scholhamer discloses the computer system of claim 42, further comprising: means for setting a master mode bit in another bus interface logic; and means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

As per claim 44, Scholhamer discloses the computer system of claim 42, further comprising: means (301) for rejecting (retry) an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 45, Scholhamer discloses the computer system of claim 42, further comprising: means for resetting the master mode bit; and means for flushing buffers of the bus interface logic in response to resetting the master mode bit.

As per claim 46, Scholhamer discloses the computer system of claim 45, further comprising: means (Node bridge) for accessing the bus interface logic in response to making an

attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (uncached; col. 12, lines 14-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 16-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriarty et al. (USPN 6,446,149; Moriarty) in view of Kao et al. (USPN 6,651,168; Kao).

As per claims 16 and 17, Moriarty discloses the claimed invention except for the master device comprises a crypto processor and security hardware. Kao teaches authentication framework for multiple authentication processes and mechanisms to enable a computer system to authenticate a user with a selected one of the plurality of authentication processes (Abstract). It

would have been obvious to one of the ordinary skill in the art at the time of the invention to incorporate the teachings of Kao in the Moriarty system as taught by Kao. In doing so it would provide flexibility in providing diverse user authentication mechanisms and processes for a stand-alone computer system of for a distributed computer network (col. 2, lines 45-54).

As per claims 18, 21, 28 and 29, Moriarty discloses the claimed invention including a master device (busmaster); at least a first bus interface logic (bridge) coupled to the master device, wherein the first bus interface logic comprises a first storage location (address space/ semaphore memory cell) for storing a first master mode bit; and at least a second bus interface logic (bridge) coupled to the device, wherein the first bus interface logic (bridge) comprises a second storage location (semaphore memory cells) for storing a second master device mode bit; wherein the master device is configured to cause to be set the first master mode bit in the first storage location and the second master mode bit in the second storage location; wherein the first bus interface logic is configured to exchange data only between the master device and the second bus interface logic when the first master mode bit is set; and wherein the second bus interface logic is configured to exchange data only between the device and the first bus interface logic when the second master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 10, lines 21-67; col. 11, lines 35-46; col. 12, lines 52-56). Moriarty does not disclose a device, different from the master device, configured to provide authentication data to the master device and a cryptoprocessor and security hardware.

Kao teaches authentication framework for multiple authentication processes and mechanisms to enable a computer system to authenticate a user with a selected one of the plurality of authentication processes (Abstract). It would have been obvious to one of the

ordinary skill in the art at the time of the invention to incorporate the teachings of Kao in the Moriarty system as taught by Kao because this would provide flexibility in providing diverse user authentication mechanisms and processes for a stand-alone computer system of for a distributed computer network (col. 2, lines 45-54).

As per claim 19, wherein the master device is configured to set and reset the first and second master mode bits (Moriarty; read/write; col. 8, lines 18-67).

As per claim 20, wherein the first and second bus interface logics are further configured to flush output buffers in response to the first and second master mode bits being reset (Moriarty; write; col. 9, lines 44-51 and col. 11, lines 35-46).

As per claim 22, wherein the first and second storage locations are configured t store one or more addresses, and the first and second bus interface logics are configured to exchange data only with one or more addresses as stored therein (Moriarty; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 23, wherein the one or more addresses comprise an address range, wherein the first and second bus interface logics are configured to exchange data only within the address range (Moriarty; e.g. col. 11, lines 20-25).

As per claim 24, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits (Moriarty; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 25, wherein the first and second storage locations are further configured to store one or more addresses, and wherein the first and second bus interface logics are each

configured not to exchange data with the one or more addresses stored therein (Moriarty; e.g. col. 9, lines 44-47).

As per claim 26, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits (Moriarty; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 27, a processor configured to exchange data through the first and second bus interface logics when the first and second master mode bits are not set; and wherein the first and second bus interface logics are each further configured not to exchange data for the processor when the first and second master mode bits, respectively, are set. The limitation would be within the inherent teachings of Moriarty in that in the Moriarty system when the master mode bits are not set, normal data transfer over the bus through the bridges can take place. However, when the master mode bits are set, only the bus master(s) with exclusive access can exchange data through the bridge.

(11) Response to Argument

In regards to applicants argument that Moriarty, Parks, and Scholhamer do not describe or suggest a master mode bit, i.e. a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system, as defined in the patent application: The closest the examiner could find of this "definition" of a master mode bit in the specification is "The method 4800 shown in FIG. 37 includes transmitting a master mode

signal to one or more bus interface logics or other devices that include a master mode register, in block 4805. The method 4800 also includes setting a master mode bit in the master mode register of each of the one or more bus interface logics or other devices that includes the master mode register to establish a secure transmission channel between the master mode logic and the data input device, in block 4810. The master mode logic and the data input device exchange data outside the operating system of the computer system through the bus interface logics or other devices that include the master mode register". The examiner notes the last sentence was about the master mode logic not the master mode bit. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim language states "A bus interface logic configured with a storage location configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set." Thus this master mode bit is clearly a semaphore. A semaphore is defined in Microsoft press computer dictionary as "a signal, a flag variable, used to govern access to shared system resources. A semaphore indicates to other potential users that the file or other resource is in use and prevents access by more than one user." Thus a semaphore is a bit that is set in one or more interface logics or other devices that include the semaphore storage location to establish a secure transmission channel between the interface logic and the data input device.

The examiner notes the claim language does not even mention an operating system or master mode logic that operates outside the operating system. Thus pointing out that the master

mode bit operates outside the operating system introduces an operating system that is never claimed, and introduces operating outside said unclaimed operating system. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The examiner again sees no difference between a semaphore and the claimed master mode bit. "Modern claim practice requires that the claims stand alone to define the invention" *Ex parte Fressola* 27 USPQ2d 1608 (Bd. Pat. App. & Inter. 1993) at 3.

Further the examiner notes that both Moriarty et al and Scholhamer et al set their semaphore outside any operating system. This is immaterial to the claim language however the examiner wanted to point out these references even comprise applicants unclaimed argued feature.

In regards to applicants argument that the examiner alleges that the feature upon which the applicant relies are not recited in the rejected claims: Since the claim language does not require an operating system or master mode logic the previous examiner was correct in concluding that the applicant is relying on features which are not claimed.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there

is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

The test of obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," *In re Gorman*, 933 F.2d at 986, 18 USPQ 2d at 1888.

> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ 2d 1500, 1502 (Fed. Cir. 1988).
>
> "Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).
>
> "In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found *in* a specific reference."
>
> Entire quote from *In re Oetiker*, 24 USPQ 2d 1443 (CAFC 1992).

Accordingly, it is not required to disclose or specifically suggest particular elements. Instead the measure is what the teachings would suggest to one of ordinary skill in the art, not what the art specifically suggests.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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